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# High-speed CMOS DD amplifiers at low static current consumption

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***Abstract*—this paper presents design technique for linear operation range of CMOS differential difference amplifier with the primitive object of the Trans conductance on its Differential stage corner voltage ($V_{cn}$), is considered. The mathematical and comparative SPICE modeling results of typical CMOS Differential difference stage on the channel width of CMOS transistors at different static currents are presented using Mentor graphics 0.25micro Technology. The DDA can be reconfigured as an operational amplifier, this novel implementation brings significant reduction in static current to pace slew rate of the output voltage (SR).**

***Keywords*—CASCODE current mirror;Differential difference amplifier; corner voltage (Vcn); unity gain buffer; slew rate.***

## • INTRODUCTION

In recent years wireless communication systems dominated the telecommunication era. Consequently high speed, low power consumption, power delivered to the load and area efficient mixed/analog signal processing circuits became essential. Circuits like filters, mixers, registers and variable gain amplifiers are common parts in any communication system hardware. These blocks were realized using voltage op-amps. However, voltage op-amp based circuits cannot operate adequately for high frequency applications due to their constant gain bandwidth product. The development of new active blocks that consume less power and consumes small area in addition to their suitability for high frequency applications became a must. Research efforts were directed to two different method Differential stages. One method was to introduce low power current-mode active blocks suitable for high frequency applications like current conveyors. The other method was to modify the voltage op-amps structure in order to improve their frequency response and reduce the area of the overall system.

The classical operational amplifiers (Op-Amps) are well researched and are widely used for designing analog devices. However, due to a number of known limitations related to the characteristics of the Op-Amps architecture, today we are searching for other alternative analog active elements [1]. Among them is a Differential difference operational amplifier (DDOA) [2-3], which has a number of indisputable advantages in comparison with a typical Op-Amp.

The Differential difference operational amplifier (DDOA) is rather new functional assembly of analog micro circuitry [1] and has specific connection circuits. In spite of a number of the unique characteristics it is random used in instrument making. The designing of DDA based on the bipolar and field effect technological processes which provide the radiation hardness of the circuits at the absorbed dose up to 1millirad and neutron flux up to 1013 n/cm2 is of great Current interest.

One of the requirements for the input stages of Differential stage 1, differential stage2 DDOA Fig. 1 - extended range of linear operation[6] based on biasing. In this case, the corner voltage of the pass-through characteristic $I_{out} = f(V_{inp})$ of the input Differential Stage ($V_{cn}$) should be commensurate with the supply voltage. If this condition is not met, then the efficiency of the use of DDOA in analog interfaces deteriorates significantly. In this case, the basic equations DDOA [4] for linear operation are violated. This leads to Differential stage to the dependence of the effective voltage transfer coefficient in typical switching schemes from the signal amplitude and nonlinear distortions.

The purpose and novelty of this article is to develop recommendations for the design of a CMOS DDOA taking into account low static current consumption of input stages and parameters of CMOS field-effect transistor processes by 0.25micro CMOS, using SPICE environment.

## • EXISTING METHOD

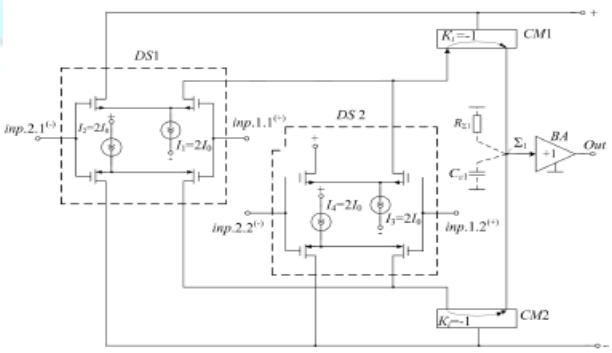


Fig.1.CMOS DDOA functional blocks

### ○ *NONLINEAR MODE OF DDOA*

We first obtain the basic equations for switching on the DDOA of Fig. 1 in the diagram of the instrumental amplifier Fig. 2 for large loop gain and 100% negative feedback, when resistor R1 = 0.

When input voltage vin.1 of Differential Stage1 relatively small ($V_{in1} < V_{cn}$) [6] based on biasing, in the circuit of Fig. 2 manifested all the advantages of the DDOA.

$$v_{out} = \frac{K_{BA}R_{\Sigma}g_{m1}}{1+K_{BA}R_{\Sigma}g_{m2}}v_{in1} \approx v_{in1}, \qquad (1)$$

Where KBA is the voltage transfer coefficient of the buffer amplifier BA; RΣ - equivalent resistance at the high impedance junction Σ1; gm1=gm2transmission conductivity Differential Stage1 and Differential Stage2, depending on the angle of Inclination of the flow characteristic $i_{out} = f(VIN)$.

- PRAPOSED METHOD

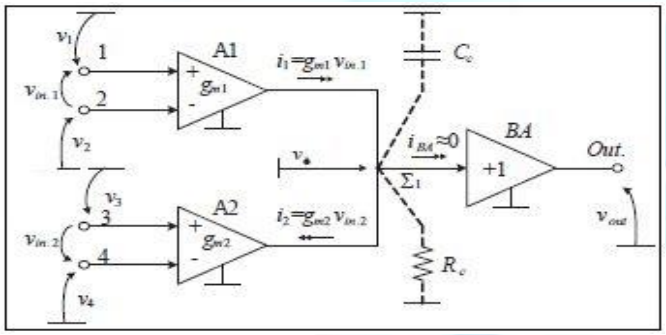


Fig.2. The functional Circuit of DDOA

In the circuit of Fig. 2 with the introduction of the feedback resistor (R1, R2) and KBARΣgm2>>1there is a possibility of digital control of the transmission coefficient, because,

$$v_{out} \approx v_{in}\left(1+\frac{R_1}{R_2}\right). \qquad (2)$$

The Differential Stage1 is supplied with an input signal with large amplitude greater than Vcn (Vin1≥ Vcn)[6] based on biasing, the output voltage in the switching circuit Fig. 2 does not depend on the vin.1 and limited to level.

$$V_{out.max} \approx V_{lim}\left(1+\frac{R_1}{R_2}\right). \qquad (3)$$

### ○ *Computer simulation of DD amplifier using Mentor graphics.*

Differential difference amplifier [4] comprised by 1.Current mirror,[4] 2.Diffrental amplifier (Differential Stage1), 3.Differential amplifier (Differential Stage2), 4.Buffer amplifier [4] (BA).

1.Current mirror is established to maintain current stability in whole circuit, it has MN1as source and MN2 as a mirror transistor and ammeter as a test point to measure mirror current, and which consumes less power because of its architecture nature.

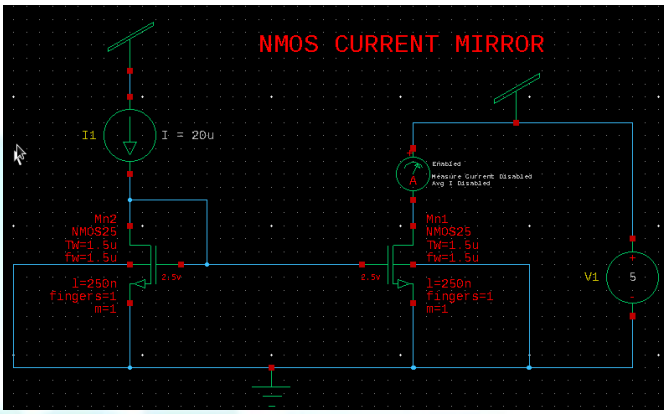


Fig.3. Current mirrors with 20µAms.

2. Differential amplifier

Basic building blocks of Differential Stage1 amplifier has MN3 as a Vin11,MN4 as aVin12, and Two MP1,MP2 are provided proper biasing for Differential Stage1,Which amplifies the difference of the input stages. Basic building blocks of Differential Stage2 amplifier has MN5 as a Vin21,MN6 as aVin22, and Two MP1,MP2 are provided proper biasing for Differential Stage2,Which amplifies the difference of the input stages.

In this architecture we are providing signals on Vin11 (Differential Stage1) and Vin21 (Differential Stage2) to make both amplifiers as inverting amplifiers.

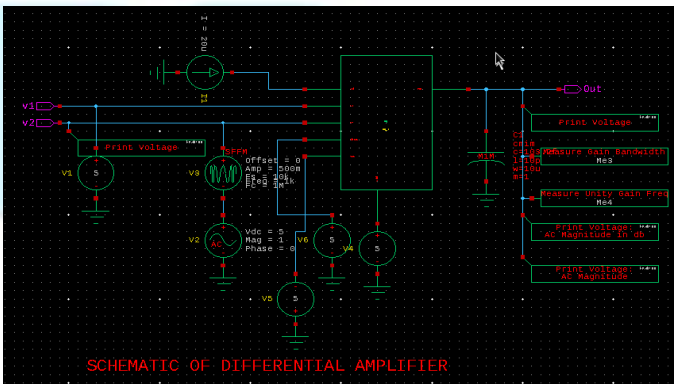


Fig.4. Differential Amplifiers.

The below figure shows the simulation results of Differential Stage1 producing gain of 23.76dB with output voltage of15.35 volts.

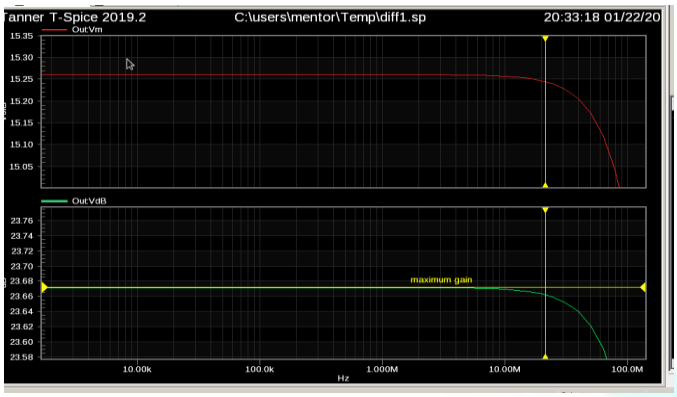


Fig.5. Differential amplifier gains with phase.

The below figure shows final DDOA with BA.BA stage constructed with common drain amplifier.

To get output simulation results we need to apply SPICE elements to the proper biased circuit, SPICE models are provides print voltage in magnitude, gain in dB, phase shift.

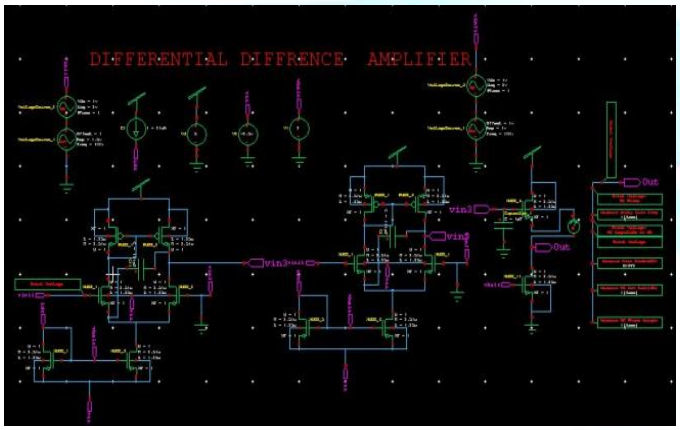


Fig.6. DDOA final schematic.

The below figure shows computer simulation results of DDOA in which static current measured with ammeter which is in mA range, when it is operated in linear region of operation.

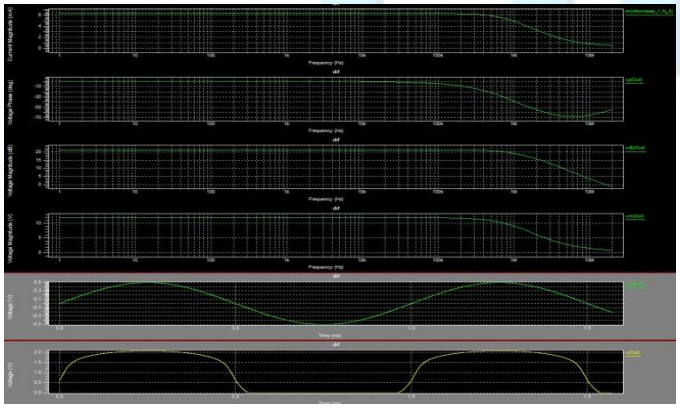

Fig.7. DDOA simulation results in linear region of operation.

The slew rate is depends on Differential stage on the changing of capacitor, the values shown in below Table.

Table.1. Capacitance V/s Slew rate

| Capacitance of capacitor cc1 | Previous -SR V/us | Present -SR V/us |
|---|---|---|
| 1PF | 46.5 | 1500 |
| 3PF | 54.4 | 500 |
| 10PF | 190 | 302 |
| 100PF | 300 | 1683.3 |

- DESIGN RULES AND LAYOUTS

As the length between the source and drain is 250nm or channel length, [5] we are using 250nm Technology.

Table.2. PMOS design rules.

| PMOS | | | |
|---|---|---|---|
| S.NO | FIELD COMPONENTS | LENGTH | WIDTH |
| 1. | N-WELL | 2.995 | 4.110 |
| 2. | SUBSTRATE | 1.050 | 1.050 |
| 3. | P IMPLANT | 2.005 | 2.065 |
| 4. | GATE | 2.100 | 0.250 |
| 5. | METAL | 1.140 | 0.545 |
| 6. | GROUND | 4.170 | 0.645 |

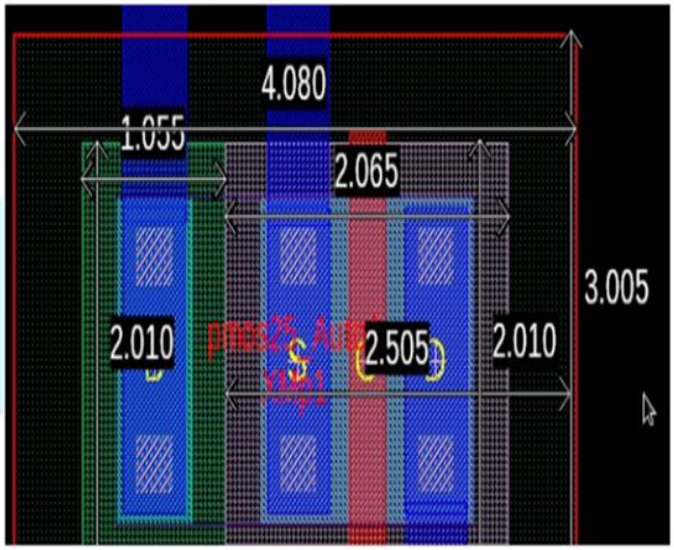


Fig.8. Design rules for PMOS

This based on the rules offered by mentor graphics 250nm technology libraries [5].

Table.3. Design rules for NMOS.

| NMOS | | | |
|---|---|---|---|
| S.NO | FIELD COMPONENTS | LENGTH | WIDTH |
| 1. | P-WELL | 2.045 | 2.000 |
| 2. | SUBSTRATE | 1.990 | 1.010 |
| 3. | N IMPLANT | 1.550 | 1.495 |
| 4. | GATE | 2.095 | 0.250 |
| 5. | METAL | 3.710 | 0.625 |

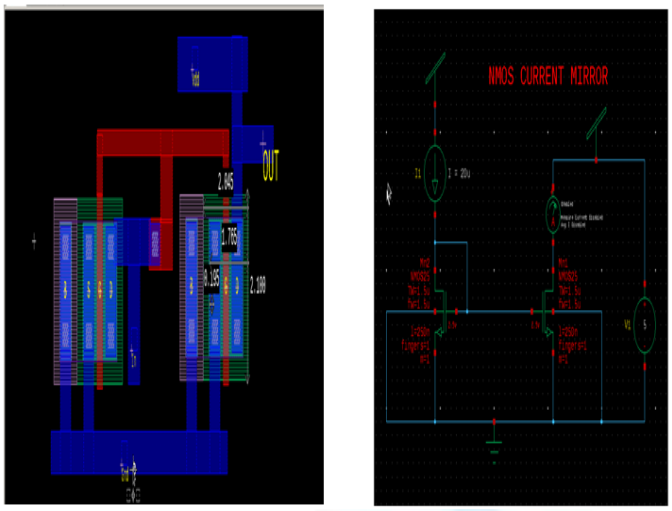


Fig.9. Design rules for NMOS and PMOS

The rules are based on the rules offered by mentor graphics 250nm technology libraries [5].

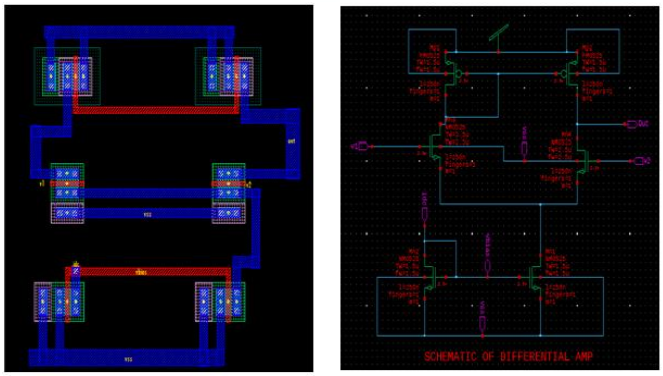


Fig.10. Design rules for Differential Stage1 or Differential Stage2.

NMOS and PMOS design rules based on the rules offered by mentor graphics 250nm technology libraries [5].

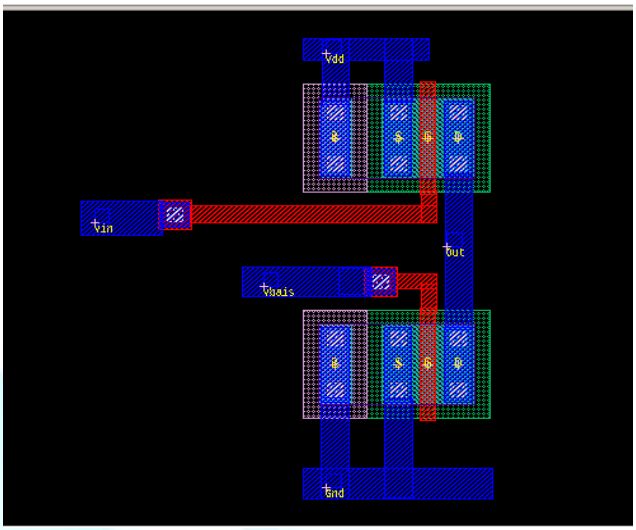


Fig.11. Design rules for Buffer Amplifier.

NMOS and PMOS layout rules based on the rules offered by mentor graphics 250nm technology libraries [5].

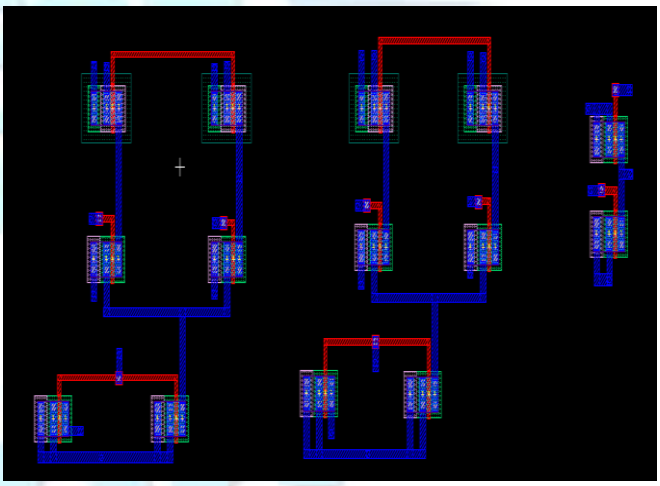

Fig.12. Design rules for DDOA.

NMOS and PMOS design rules based on the rules offered by mentor graphics 250nm technology libraries [5].

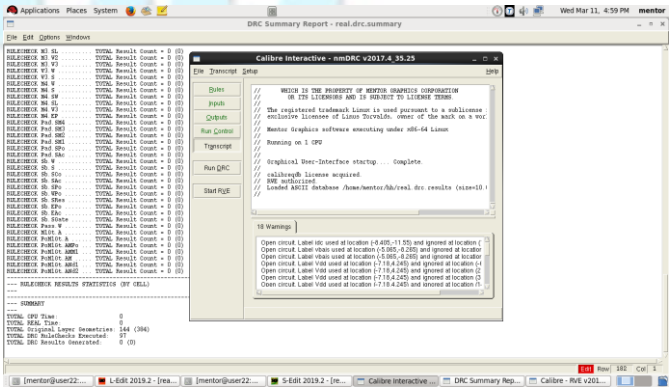

Fig.13.Design rule check (DRC) report by CALIBRE tool

## V. CONCLUSION AND TO BE RESEARCH

The apparent simplicity of construction and Application of DDOA is associated with the need to further improve their circuit design and exclude non-linear operating modes. When designing a CMOS DDOA, it is necessary to take into account the significant influence of the static mode, as well as the length and width of the channel of CMOS transistors on the range of linear operation of the input stages. The use of differentiation correction circuits in each input stage of the CMOS DDOA allows increasing the maximum slew rate of the output voltage of the DDOA with limitations on the static current of the input stages to analyses these we need apply fault injection at each stage. So to analyze CMOS DDOA further by injecting fault models and test their performance by IDDQ (current direct drain quiescent) and IDDT current direct drain transient) method Differential stage.

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